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Damage-Free Back Channel Wet-Etch Process in Amorphous Indium–Zinc-Oxide Thin-Film Transistors Using a Carbon-Nanofilm Barrier Layer

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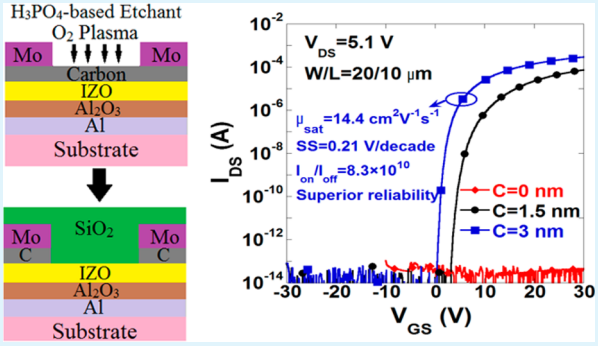
Supporting Information

ABSTRACT: Amorphous indium–zinc-oxide thin film transistors (IZO-TFTs) with damage-free back channel wet-etch (BCE) process were investigated. A carbon (C) nanofilm was inserted into the interface between IZO layer and source/drain (S/D) electrodes as a barrier layer. Transmittance electron microscope images revealed that the 3 nm-thick C nanofilm exhibited a good corrosion resistance to a commonly used H_3PO_4-based etchant and could be easily eliminated. The TFT device with a 3 nm-thick C barrier layer showed a saturated field effect mobility of 14.4 $cm^2 V^{-1} s^{-1}$, a subthreshold swing of 0.21 V/decade, an on-to-off current ratio of 8.3×10^{10}, and a threshold voltage of 2.0 V. The favorable electrical performance of this kind of IZO-TFTs was due to the protection of the inserted C to IZO layer in the back-channel-etch process. Moreover, the low contact resistance of the devices was proved to be due to the graphitization of the C nanofilms after annealing. In addition, the hysteresis and thermal stress testing confirmed that the usage of C barrier nanofilms is an effective method to fabricate the damage-free BCE-type devices with high reliability.



KEYWORDS: *thin-film transistors, amorphous-oxide semiconductor, back-channel-etch, carbon nanofilm*

INTRODUCTION

Amorphous oxide semiconductors (AOSs) based thin-film transistors (TFTs) have received much attention as promising candidates in future display applications due to its high mobility, good uniformity, and excellent electrical stability.[1−4] Moreover, the possibility of a low-temperature process makes AOS-based devices compatible with flexible substrates and can possibly facilitate the extended application to flexible devices such as displays, biosensors and memories.[5−8]

Theoretically, it is possible to utilize the current amorphous Silicon (α-Si) TFTs mass-production line to fabricate the AOS-TFTs due to their similar device structures. However, it is a challenge to patterning the source/drain (S/D) directly on the AOS layer (back-channel-etch, BCE), because the AOS materials are very susceptible to most commonly used etchants and plasma treatment employed in wet-etch and dry-etch processes, respectively.[4,9−13] By inserting an etch stopper layer between the AOSs and source/drain (S/D) electrodes, denoted as etch-stopper layer (ESL) structure, the impact on the active layer during the patterning of the S/D can be greatly reduced. Recently, AOS-TFTs with ESL structure have shown excellent uniformity and stability for display demos. However, the ESL structure not only increases the production cost because an additional photolithography process is inevitably required but also leads to the difficulty in the scale-down of TFT dimension due to the necessary overlapped regions.[13] Therefore, the achievement of high-performance AOS-TFTs based on the BCE structure using a relatively low-cost and damage-free fabrication process is drawing researchers' attentions.[13−15] Recently, we used an H_2O_2-based etchant for etching the S/D metal and employed a postplasma treatment to realize high-performance amorphous In–Zn–O (IZO) TFTs with BCE structure.[16,17] It is worth noting that amorphous IZO film is widely recognized as a potential active-layer candidate in AOS-TFTs due to its high mobilities and good performance.[18,19] However, the use of H_2O_2-based etchant introduces two disadvantages: (1) it has a short shelf life; (2) especially, the H_2O_2 content has a possibility of explosion, so it is difficult to

Received: March 26, 2014
Accepted: June 27, 2014
Published: June 27, 2014

utilize the H_2O_2-based etchants in the mass-production process. On the other hand, a barrier layer inserted into the interface between the active layer and S/D metal was employed to fabricate the AOS-TFTs with BCE structure. Generally, the barrier layer should provide a good protection to the AOSs layer during the S/D etching and have no negative effect on TFT performance. Recently, ultrathin Titanium oxide (TiO_x) film has been reported as a barrier layer to achieve the BCE structure.[20] However, the TiO_x has a chance to react with AOSs at the interface of back channel, which may lead to increase of instability of TFT performance. Alternatively, graphene is a good candidate for the prevention of interfacial reaction or interdiffusion at the interface due to the high chemical stability.[21] Nonetheless, it is difficult to deposit a larger area graphene film, which limits graphene to applications in the mass production of flat-panel displays (FPD).

In this work, an amorphous carbon (C) nanofilm fabricated using conventional sputtering method was inserted into the interface between IZO and S/D electrodes as a barrier layer. We found that the C nanofilm is robust enough to protect IZO channel from etching during the formation of the S/D electrodes using an H_3PO_4-based etchant. The H_3PO_4-based etchant composed of phosphoric acid, acetic acid, water, and additive nitric acid, is conventionally used for etching aluminum (Al) and molybdenum (Mo) in the semiconductor industry. The IZO-TFTs fabricated with the C barrier layer showed superior TFT performance and good stability under bias thermal stress.

EXPERIMENTAL SECTION

Device Fabrication. Figure 1 shows a schematic representation of the key steps involved in the fabrication process. A 300 nm-thick Al as gate metal was deposited onto glass substrates by DC sputtering and patterned by wet etching. Subsequently, the film was anodized in an electrolyte consisting of 3.68 wt % ammonium tartrate solution and ethylene glycol, forming a 200 nm-thick layer of Al_2O_3 on the surface of the Al.[22] A 30 nm-thick IZO was deposited on the anodic oxide film by radio frequency (RF) magnetron sputtering, followed by wet etching in diluted hydrochloric acid. During the IZO deposition, the flow rates of Ar and O_2 were kept at 50 and 4 sccm, respectively, and the power was fixed at 500 W. For the S/D electrodes, a stacked structure of C (1.5 or 3 nm)/Mo (200 nm) was sequentially formed by sputtering. Then, a commonly used H_3PO_4-based etchant and oxygen (O_2) plasma were employed to pattern the Mo and C film, respectively.[12−17] Finally, the devices were passivated by a 300 nm-thick SiO_2 layer formed by plasma enhanced chemical vapor deposition (PECVD). All the devices were defined with channel width/length of 20/10 μm and were annealed in air at 300 °C for 30 min.

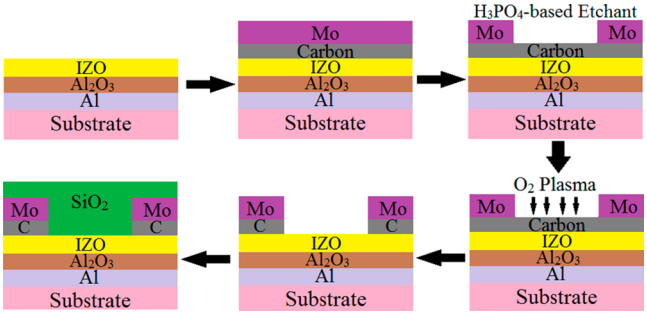


Figure 1. Schematic illustration of the key steps involved in the fabrication of staggered bottom gated BCE-TFT. A carbon barrier film was inserted between Mo S/D and IZO channel.

Electrical Characterization and Measurement Conditions. The electrical characteristics of the devices were measured by using a probe station and a semiconductor parameter analyzer (Agilent B1500). The field-effect mobility (μ) is calculated from a linear fitting to the plot of the square root I_{DS} versus the V_{GS} in saturated operation region. The subthreshold swing (SS) is taken as the minimum value of $(d \log (I_{DS})/d V_{GS}))^{-1}$, and the threshold voltage (V_{th}) is defined at constant drain current I_{DS} of $W/L \times 10$ nA. The thermal stress (TS) was performed from room temperature (RT) to 120 °C in dark state. For the positive bias thermal stress (PBTS) and negative bias thermal stress (NBTS) experiments, a V_{GS} of +20 and −20 V was applied, respectively, and a V_{DS} of 0 V was maintained at a substrate temperature of 80 °C for each device. The maximum stress duration was 7200 s. During the stress experiment, transfer curves were collected at the V_{DS} of 9.1 V.

Carbon Nanofilm Characterization. The quality of the C nanofilms was investigated by Raman spectroscopy (Horiba Jobin Yvon, Aramis) and current−voltage measurements. The effect of the C nanofilms on the protection for AOS in the back-channel-etch process was analyzed via polarizing microscope, transmittance electron microscope (TEM, JEOL JEM2100F), and X-ray photoelectron spectroscopy (XPS, Thermo Scientific K-Alpha). The element distributions relevant to C nanofilms on actual device were depicted by using high-energy reflection electron energy-loss spectroscopy (EELS, Gatan).

RESULTS AND DISCUSSION

Characteristics of Carbon Nanofilm. Figure 2a,b shows the Raman spectra of as-deposited and annealed (at 300 °C for 30 min) C nanofilms, respectively. The wavelength of excitation laser was 514 nm. A broad peak composed of G and D peaks is observed. The G peak around at 1500−1630 cm^{-1} involves the in-plane bond-stretching motion of pair of carbon sp^2 atoms, whether in C═C chains or in aromatic rings. Relatively, the D peak around 1400 cm^{-1} is breathing mode of those sp^2 sites.[23−25] But this mode is forbidden in graphite crystal and only becomes active in the presence of disorder.[25] The positions of G peak and D peak, the ratio of I_D to I_G (I_D/I_G), and the full width at half-maximum (fwhm) were extracted and listed in Table 1. It can be seen that both the samples exhibit a large fwhm in the G and D peaks, which suggests that the C nanofilms deposited by sputtering is amorphous and highly disorder. As previous reports,[23−25] in the amorphous C film, the shift of G-peak position toward higher frequency and the increase in I_D/I_G indicate that the number of the aromatic rings increases. Therefore, we speculate that the more ordered phases would be formed in the amorphous C nanofilms by introducing the annealing. The current−voltage characteristics of the C nanofilms are plotted in Figure 2c,d. In the measurement, planar Mo electrodes with different distances were fabricated by lithography method on the surface of the C nanofilms. Resistance can be extracted from the current−voltage curves multiplied with the width of electrode (W) against the distance (L) of two electrodes. The resistivity of as-deposited and annealed amorphous C nanofilms deduced from the transfer line model (TLM) were 1.1 and 0.1 Ω·cm, respectively, which coincided with that of reported α-C films.[26] The decrease of resistivity can be explained by the graphitization of α-C nanofilms after annealing.[27]

In order to investigate the effect of the C nanofilms on the protection for AOS in the back-channel-etch process, stack configurations of Mo (200 nm)/C/IZO (30 nm) with various C thicknesses were prepared. The C nanofilms and Mo were

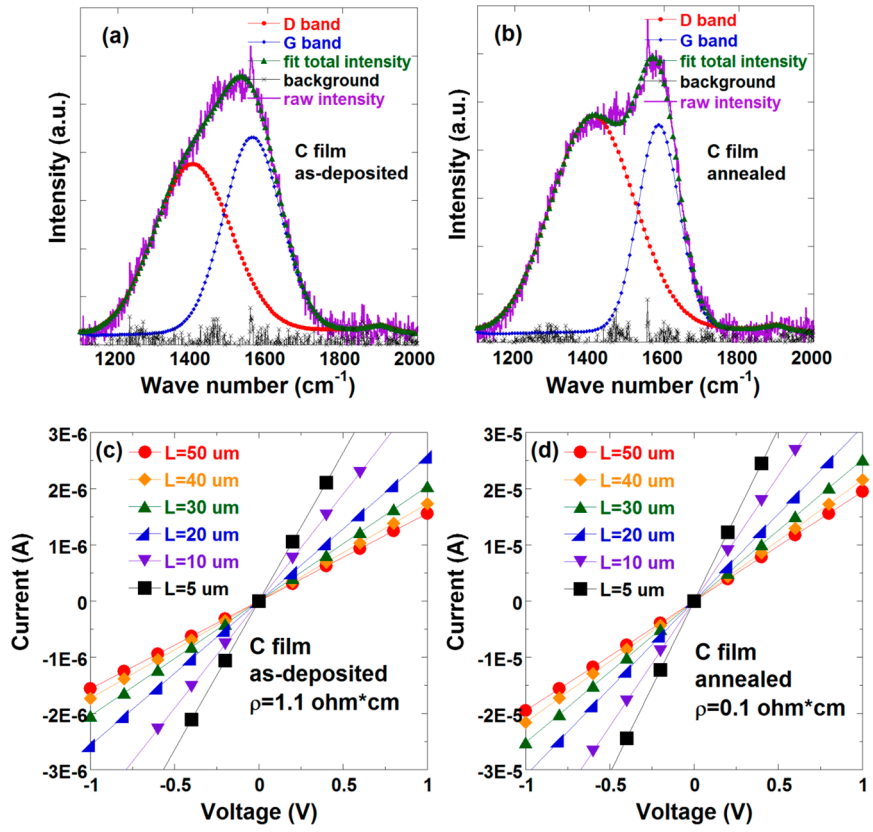


Figure 2. Raman spectra of (a) as-deposited and (b) annealed C nanofilms on Si wafers. Current–voltage characteristics of (c) as-deposited and (d) annealed C nanofilms on glass substrates, the annealed C nanofilms were annealed at 300 °C for 30 min.

Table 1. Summary of the Positions of D Peak and G Peak, the Ratio of I_D to I_G (I_D/I_G), and the Full Width at Half Maximum (FWHM) of the D Peak and G Peak

carbon film	D peak	G peak	I_D/I_G	fwhm of D peak	fwhm of G peak
as-deposited	1399	1559	1.16	241	180
annealed	1408	1585	2.15	262	128

deposited sequentially onto the patterned IZO film. Then the stack films were immersed in the H_3PO_4-based etchant for 3 min to form the pattern of source/drain. Figure 3 shows the polarizing microscope images of the patterned stack configurations with C thicknesses of 0, 1.5, and 3 nm, respectively. As shown in Figure 3a, the IZO film was completely etched away by the H_3PO_4-based etchant without C-nanofilm protection. On the other hand, it shows that 1.5 nm-thick C nanofilm also cannot efficiently protect the active layer, leading to the discontinuity of the nanofilm. However, the C nanofilm thicker than 3 nm demonstrates a good protection for the IZO film from attacks by the H_3PO_4-based etchant.

Electrical Characteristics of C-Barrier IZO-TFTs. Figure 4a shows the output characteristics (I_{DS} versus V_{DS}) of the IZO-TFTs prepared with different C barrier thicknesses between IZO channel and Mo S/D. It shows steep raises of I_{DS} at low V_{DS}, indicating that those devices have good ohmic contact properties. Meanwhile, it can be seen that the device with 3 nm-thick C barrier layer had much higher saturated output drain current (I_{DS}) than that of the device with 1.5 nm-thick C barrier layer under same V_{DS} and V_{GS}. The corresponding transfer characteristics of the IZO-TFTs are shown in Figure 4b. It can be seen that the IZO-TFT without C barrier layer exhibited no

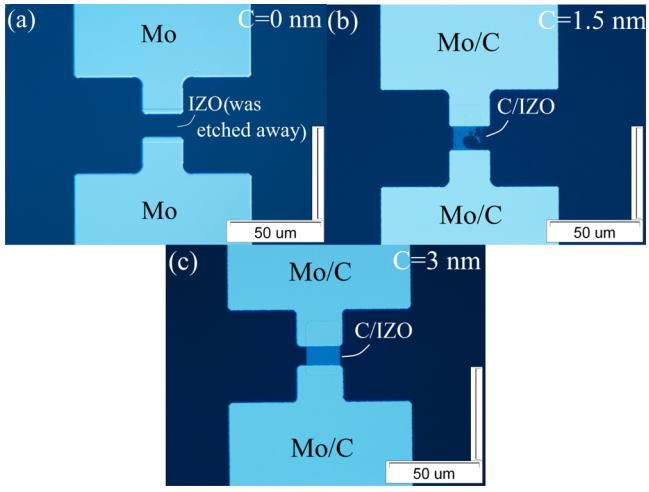


Figure 3. Polarizing microscope images of the Mo/C/IZO stack configurations while carbon nanofilm thicknesses at (a) 0, (b) 1.5, and (c) 3 nm after patterning the Mo films at a H_3PO_4-based etchant.

TFT performance, because the amorphous active layer was etched by Mo etchant during patterning of S/D electrodes. On the other hand, the device with 1.5 nm-thick C barrier layer also has inferior transfer characteristics, which can be attributed to the damage of IZO layer caused by the H_3PO_4-based etchant, just as shown in Figure 3b. Table 2 records the device parameters extracted from the transfer characteristics in Figure 4b. The saturated field-effect mobility (μ_{sat}) is calculated from a linear fitting to the plot of the square root I_{DS} versus the V_{GS} in saturated operation region. The subthreshold swing (SS) is

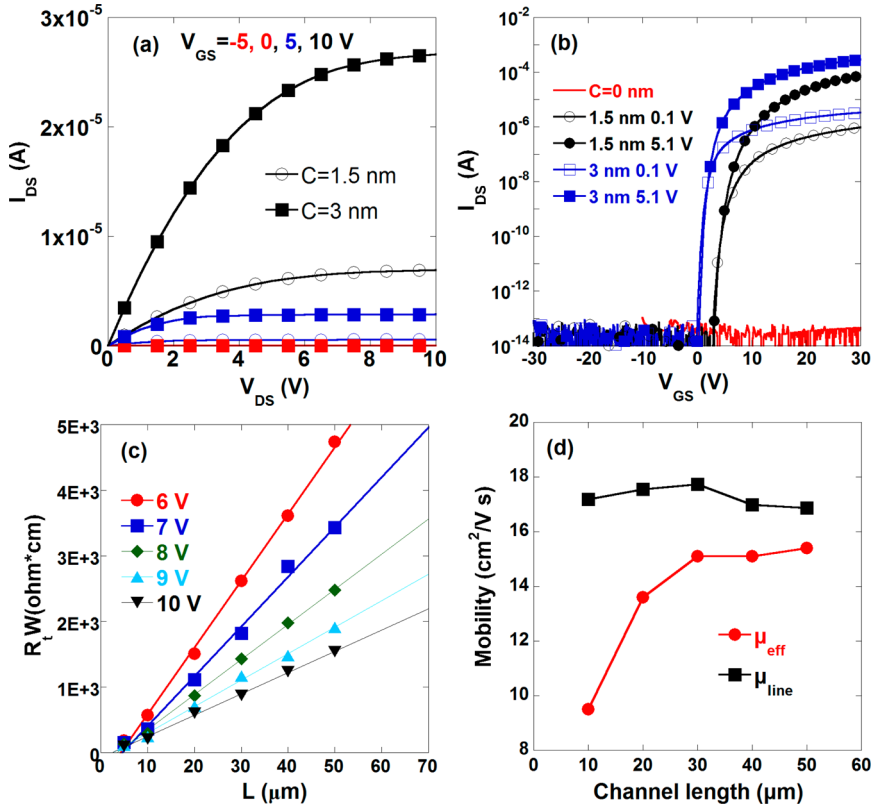


Figure 4. Output characteristics (a) and transfer characteristics (b) of the IZO-TFTs with different C barrier thicknesses between S/D electrodes and IZO channel. (c) Dependence of R_tW on L for the IZO-TFT with 3 nm-thick C barrier layer. (d) Variations of μ_{eff} and μ_{line} as a function of L for the IZO-TFT with 3 nm-thick C barrier layer.

Table 2. Device Parameters Extracted from the Transfer Curves in Figure 4b, Including Saturated Field-Effect Mobility (μ_{sat}), Sub-Threshold Swing (SS), on-to-off Current Ratio (I_{on}/I_{off}), Threshold Voltage (V_{th}), Width-Normalized Contact Resistance (R_cW), and the Value of V_{th} Shift (V_{th}) under PBTS and NBTS, Respectively

carbon film	μ_{sat} ($cm^2\ V^{-1}\ s^{-1}$)	SS (V/decade)	I_{on}/I_{off}	V_{th} (V)	R_cW Ω·cm	ΔV_{th} (P/NBTS) (V)
1.5 nm	2.7	0.30	2.0×10^9	6.1		2.9/-0.3
3 nm	14.4	0.21	8.3×10^{10}	2.0	80	0.4/-0.1

taken as the minimum value of $(d \log (I_{DS})/dV_{GS}))^{-1}$, and the threshold voltage (V_{th}) is defined at constant drain current I_{DS} of $W/L \times 10$ nA. The TFT with 3 nm-thick C barrier showed a μ_{sat} of as high as 14.4 $cm^2V^{-1}s^{-1}$, a SS of only 0.21 V/decade, an on-to-off current ratio (I_{on}/I_{off}) of larger than 10^{10}, and a V_{th} of 2.0 V. Comparatively, typical values for the TFT with 1.5 nm-thick C barrier were 2.7 $cm^2\ V^{-1}\ s^{-1}$, 0.30 V/decade, 2.0×10^9, and 6.1 V for the μ_{sat}, SS, I_{on}/I_{off}, and V_{th}, respectively.

To evaluate the intrinsic properties of the IZO-TFTs using C nanofilms as barrier layer inserted into the interface between IZO layer and Mo electrodes, the contact resistances were extracted. The parasitic source-to-drain resistance R_c was evaluated using the channel resistance method with TFTs having different channel lengths.[28] The total resistance (R_t) is defined as the sum of the channel resistance (R_{ch}) and R_c by the following equations:

$$R_t = R_C + R_{ch} \quad (1)$$

$$R_{ch} = r_{ch}L_{eff} = \frac{L - \Delta L}{\mu_i C_i W(V_{GS} - V_{thi})} \quad (2)$$

where r_{ch} is the channel resistance per channel length unit, and μ_i and V_{thi} are the intrinsic mobility and the intrinsic threshold voltage, respectively. C_i is the capacitance of the gate insulator. The ΔL is the difference between the effective channel length (L_{eff}) of fabricated TFTs and the design channel length (L). In performing R_c measurements, V_{DS} is chosen as small as 0.1 V (i.e., working in linear region) to minimize the drain voltage effect. The contact characteristics of IZO-TFTs with different thicknesses of Carbon-nanofilm barrier layer were estimated by the TLM method. The dependence of width-normalized total resistance R_tW on L for TFTs with 3 nm-thick C barrier at V_{GS} of 6, 7, 8, 9, and 10 V is shown in Figure 4c. Based on eq 1, R_c and L were estimated from the intersection point of the R_tW-L straight lines. It can be seen that the IZO-TFT with the C barrier layer showed a width-normalized contact resistance (R_cW) of 80 Ω·cm, which is slightly smaller than that of IZO-TFT without the C barrier layer fabricated by dry etching (see the Supporting Information for details), indicating that very low ohmic contacts are formed in the IZO-TFTs with the C nanofilm as barrier layer. The result shows a good agreement with the analysis of output characteristics. The value of contact resistance is also comparable with that of IZO-TFTs with ESL structure reported previously.[14] By plotting the reciprocal of r_{ch} as a function of V_{GS} and fitting the results with a line, a μ_i of 13.0 $cm^2V^{-1}s^{-1}$ and a V_{thi} of 4.2 V can be deduced from the

dx.doi.org/10.1021/am501817y | ACS Appl. Mater. Interfaces 2014, 6, 11318−11325

slope and x-intercept, respectively. Moreover, the shrinkage of the channel length L = 4.5 μm was read out, implying that effective channel length is shorter than mask channel length. According to the previous reports,[29] the shorter effective channel length in AOS-TFTs should be ascribed to etch bias or lateral diffusion of source-drain dopant. The ΔL may cause the overestimated mobility especially for short-channel TFTs. We plotted the apparent linear region mobility μ_{line} evaluated using L and effective μ_{eff} using L_{eff} as a function of channel length, respectively. As shown in Figure 4d, the μ_{line} is almost constant at 17.0 $cm^2\ V^{-1}\ s^{-1}$. However, the μ_{eff} decreases obviously with decreasing the channel length, indicating that the influence of R_c (independ on the channel length) in R_t increases as L decreases; thus, a larger voltage is dropped at the source-drain electrodes for short-channel TFTs, leading to the degradation of mobility.[30] According to eq 1, the intrinsic mobility μ_i should match the μ_{eff} value of devices with a long channel since the R_c should not be of significant influence. However, it is noteworthy that the μ_i of the C-inserted IZO-TFTs with BCE structure is lower than μ_{eff} for devices with L = 50 μm, which suggests that the carbon-nanofilm barrier inserted at source-drain electrodes may have a positive impact on charge-carriers transport. Oppositely, for the IZO-TFT with a 1.5 nm-thick C nanofilm, the R_c cannot be extracted from the channel resistance method due to the larger channel parameter dispersion, which should be ascribed to the random damages in active layer.

Analysis on the Effects of C-Barrier Layer. To further investigate the effects of C nanofilms on the contact properties of IZO-TFTs and active-layer protection, respectively, a cross-sectional transmittance electron microscope (TEM) and X-ray photoelectron spectroscopy (XPS) analysis were carried out. Figure 5a shows the cross-sectional profile of the IZO-TFT with the 3 nm-thick C nanofilm. It is worth noting that the C nanofilm at the interface between active layer and S/D electrodes exhibits a good continuity without any voids or peel-off even after annealing and O_2 plasma, which implies that the C nanofilm is reliable and stable as a barrier layer. On the other hand, at the channel region, the fast Fourier transform (FFT) of the IZO film confirms that the active layer is amorphous. There is no damage observed at the back channel, indicating that the 3 nm-thick C nanofilm has a good corrosion resistance to protect IZO channel from attacks caused by the H_3PO_4-based etchant during the formation of S/D electrodes. The result is in good agreement with the observations from the optical microscope. Furthermore, the element distributions were depicted by using high-energy reflection electron energy-loss spectroscopy (EELS). Figure 5b,c shows the distributions of elements at the S/D-contact and back-channel regions, respectively. The results prove the existence of C nanofilm at the interface between IZO layer and Mo electrodes. Meanwhile, the signals of IZO and Mo do not overlap, indicating that there is no diffusion between the active layer and S/D electrodes. Moreover, no carbon signal is detected at the back-channel region, implying that the C nanofilm can be efficiently eliminated by O_2 plasma. Therefore, we speculate that the removability of C nanofilms ensures the performance of IZO-TFTs with the inserted barrier layer is not affected by pollution at the back channel.

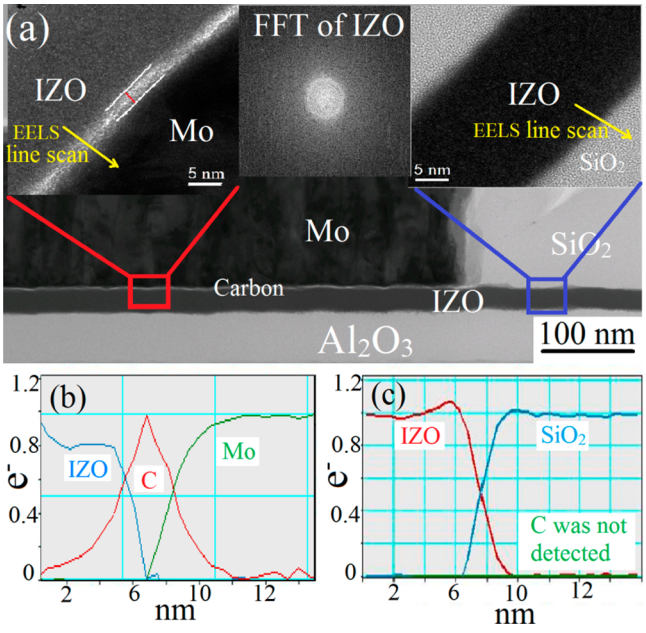


Figure 5. (a) TEM cross-section view of the IZO-TFT with a 3 nm-thick C-interlayer, the device was annealed at 300 °C in air for 30 min. HR-TEM cross section images and the corresponding FFT pattern of IZO film were in the insets of (a). EELS line scan analyses for the structures of (b) IZO/C/Mo (red rectangle in (a)) and (c) IZO/SiO_2 (blue rectangle in (a)).

Figure 6a shows the XPS spectra for C 1s at different depths of the Mo (100 nm)/C (3 nm) /IZO (30 nm)/Glass structure. It can be seen that the C 1s peak is undetectable at the outset after the surface contamination was eliminated by using Ar ions at 500 eV for 10 s. With the increase of etching time, standard C 1s peaks located at 284.3 eV are detected at the interface between Mo and IZO layer, implying only free C element existed at the interface even after annealing. On the other hand, in the case of the Mo 3d, peaks located at 227.8 and 230.9 eV are found, as shown in Figure 6b, which confirms that there is not any carbon−molybdenum bond formation and only Mo metal existed at the Mo/C/IZO interface.[31] The present results prove that C nanofilm is a stable barrier layer without reactions with Mo and IZO layer.

Reliability of C-Barrier IZO-TFTs. Hysteresis and thermal stability are the important reliability parameters in AOS-TFTs, and the behaviors were examined using the IZO-TFTs with 3 nm-thick C barrier layer in this work. As shown in Figure 7a, the forward and reverse direction transfer curves are almost identical. The drain-to-source bias voltage (V_{DS}) was 9.1 V, which is sufficiently high compared with the conventional bias voltage (~5.1 V) for device applications. Hence, the C-inserted IZO-TFTs seem to exhibit no hysteresis properties in the transfer curves between forward and reverse sweeps, indicating low defect density in the channel or at the gate insulator/channel interface.[32] It means that no defects are induced during depositing and removing the inserted C barrier layer. Figure 7b presents the evolutions of transfer curves of the IZO-TFT with a 3 nm-thick C-interlayer under thermal stress from RT to 120 °C. Surprisingly, the $I-V$ curves during TS test almost remain unchanged, except that the I_{DS} extracted from the reverse sweeping decreases with increasing temperature. According to previous reports,[33−35] in the AOS-TFTs, the V_{th} would shift toward the negative direction as increasing the temperature under TS due to the generation of thermally activated carriers from traps or defects. However, the presented results indicated that the inserted C barrier layer could improve the thermal stability of IZO-TFTs, which may be attributed to the inserted

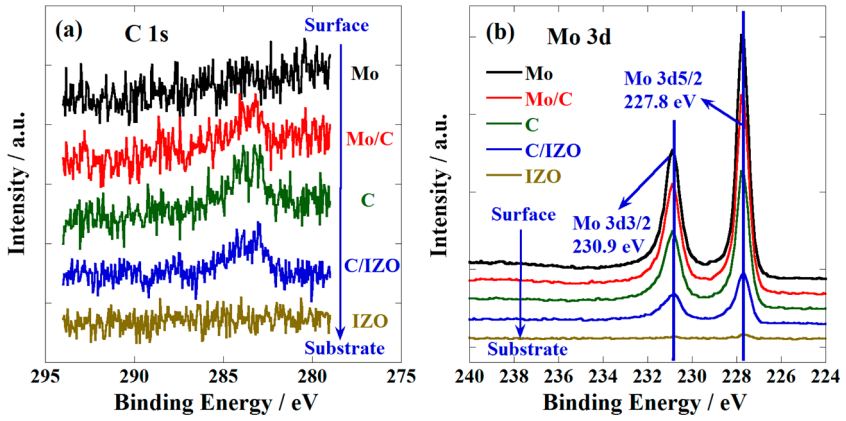


Figure 6. Depth analysis of XPS spectra of (a) C 1s and (b) Mo 3d for the Mo (100 nm) /C (3 nm) /IZO (30 nm) interface.

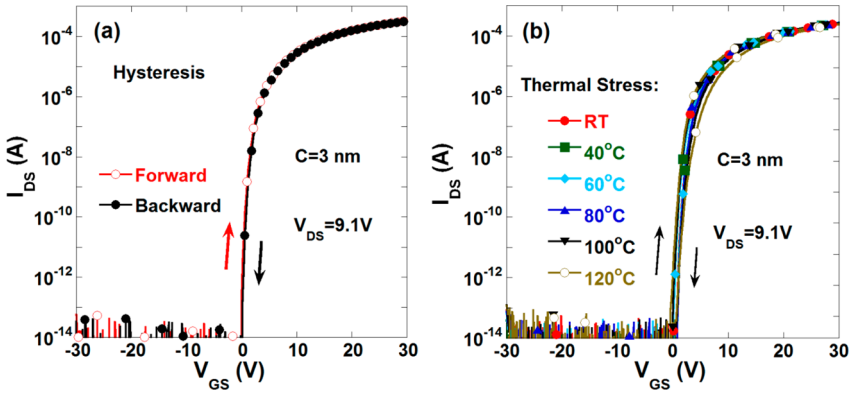


Figure 7. Transfer curves of the IZO-TFTs with 3 nm-thick C barrier layer obtained from reliability testing for (a) hysteresis and (b) thermal stress. The V_{DS} fixed at 9.1 V during measurements.

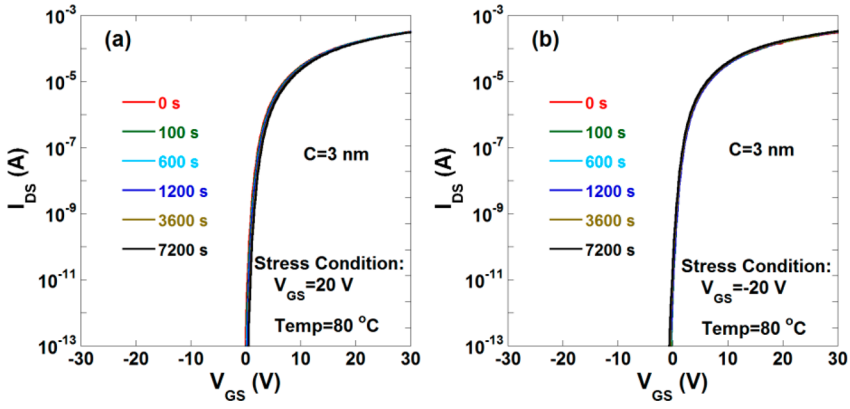


Figure 8. Variations of time-dependent transfer property under (a) PBTS and (b) NBTS for the IZO-TFT with a 3 nm-thick C-interlayer.

C barrier layer which can reduce defects generation during source/drain electrodes deposition/etching processes and further suppress the trap-induced thermal-generated holes at high temperature.

The electrical stability under gate bias thermal stress is a comprehensive test for evaluating the reliability of the BCE-TFTs. Figure 8 shows positive bias thermal stress (PBTS, V_{GS} =20 V, 80 °C) and negative bias thermal stress (NBTS, V_{GS} =-20 V, 80 °C) stability of the IZO-TFTs with 3 nm-thick C barrier layer, respectively. The result shows only V_{th} shifts of 0.4 V and less than −0.1 V under PBTS and NBTS for 7200 s, respectively. The high bias thermal stress stability is comparable to that of the IZO-TFTs with ESL structure.[36] Therefore, it confirms that the usage of C barrier nanofilms not only is an effective method to protect IZO layer from etching, but also has less impact on the TFT performance. In the case of TFTs with a 1.5 nm-thick C barrier layer, the V_{th} shifted 2.9 V and −0.3 V under PBTS and NBTS, respectively, as shown in Table 2. The inferior stability should be ascribed to the damages at the back channel of IZO.

CONCLUSION

In summary, a damage-free BCE process was achieved by introducing a C-nanofilm barrier layer. Raman spectroscopy and current−voltage measurements revealed that the annealed C-nanofilm has a lower resistivity due to the graphitization of C

nanofilm after thermal annealing. TEM images revealed that the 3 nm-thick C nanofilm deposited by sputtering is enough to protect the active layer from attacks caused by the S/D-electrodes etchant, and could be efficiently eliminated by oxygen plasma. The TFT fabricated with this method showed a saturated field effect mobility up to 14.4 cm^2 V^{-1} s^{-1}, a subthreshold swing of only 0.21 V/decade, an on-to-off current ratio of larger than 10^{10}, and a threshold voltage of 2.0 V. Moreover, the C inserted IZO-TFTs showed excellent hysteresis and thermal stress behaviors, which were proved to be due to the low contact resistance and less back-channel damages, respectively. The good bias-thermal stabilities further proved that the inserted C nanofilm could avoid the impact on the active layer during S/D electrodes formation and be inert for the TFT performance. These results indicated that the presented damage-free BCE process would be a low-cost alternation for the AOS-TFTs mass production.

■ ASSOCIATED CONTENT

Supporting Information

Associated content, including (i) adhesion tape test of the C-nanofilm, (ii) TEM line profile of the C-barrier IZO-TFT, (iii) bias stability of the IZO-TFT with a 1.5 nm-thick C-interlayer, and (iv) contact resistance of the IZO-TFT without the carbon film. This material is available free of charge via the Internet at http://pubs.acs.org.

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Funding

This work was supported by MOST (Grant Nos. 2009CB930604, 317 2009CB623600, and 2011AA03A110), NSFC (Grant Nos. 60937001, 318 61036007, and 51173049) and China Postdoctoral Science Foundation (Grant No. 2014M552197).

Notes

The authors declare no competing financial interest.

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